REMARKS

Claims 63-70 and 72-86 are pending in this application, with claims 63, 70, 73, 74, and 77-80 being independent. Claims 63-69, 72-76, 78-80, 82, and 84-86 have been withdrawn from consideration. Claims 70, 77, and 81 have been amended. Support for the present amendments may be found in the application at, for example, page 25, line 10 to page 28, line 25 and FIGS. 1A-1F. No new matter has been introduced.

For the reasons set forth below, Applicants respectfully submit that all pending claims as currently amended are patentable over the cited prior art.

Information Disclosure Statement

Applicants respectfully request that the Examiner provides Applicants with an initialized copy of the attached PTO form 1449 indicating that each of the references cited therein has been considered and made of record.

Claim Rejection – 35 U.S.C. § 103

Claims 70, 71, 77, and 83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Publication 2003/0127667 ("Inoue") in view of JP 2002-100671 ("Ishizuka"). Claim 81 was rejected under § 103(a) as being unpatentable over Inoue in view of Ishizuka and further in view of U.S. Patent Number 6,096,612 ("Houston"). Applicants respectfully traverse these rejections for at least the following reasons.

As amended, claim 70 recites a method for manufacturing a solid-state imaging device, the method includes a step (a) of forming, on the semiconductor substrate, a protection film including an opening portion that exposes the element isolation formation region and a region

located beside the element isolation formation region of the semiconductor substrate; a step (b) of forming a sidewall on a side face of the opening in the protection film; and a step (c) of forming a trench in the element isolation formation region in the semiconductor substrate by etching using the protection film and the sidewall as a mask.

The method further includes a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c); a step (e) of forming an element isolation region by burying the trench with a burying film after the step (d); and a step (f) of forming a photoelectric conversion section and an active region in the element formation regions after the step (e). In the step (c) the width of the trench is made smaller by the thickness of the sidewall than the width of the opening in the protection film, and in the step (f), due to the width of the trench narrower than the width of the opening in the protection film, the photoelectric conversion section and the active region are arranged apart from the element isolation region.

To provide context, Application describes in paragraphs [18, 19, 116, and 117] that because of the formation of the trench in the semiconductor substrate by etching on the semiconductor substrate using the protection film and the sidewall as a mask, the width of the trench can be made smaller by the thickness of the sidewall than the width of the opening in the protection film. Therefore, even in the case where the opening is formed so as to have a minimum opening width that can be patterned by the currently available technique, the trench whose width is narrower than the minimum opening width formed by patterning can be formed.

After forming the trench, an element isolation is formed by burying the trench with the burying film, thereby ensuring the element isolation power and making the element isolation miniaturized. If the width of the trench is narrower than that of the opening in the protection

film, the photoelectric conversion section and the active region are arranged apart from the element isolation region. As a result, even if thermal stress is generated in the vicinity of the trench after the trench is buried with the burying film, the leak current flowing towards the photoelectric conversion section and the active region can be reduced. In turn, the dark current and white flaws can be prevented.

Accordingly, claim 70 of the present invention can ensure miniaturization of the element isolation and prevent the dark current and white flaws.

Applicants respectfully request reconsideration and withdrawal of the rejection of claim 70 and its dependent claims because Inoue and Ishizuka, either alone or in combination, fail to describe or suggest a method for manufacturing a solid-state imaging device that includes, among other steps, a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c) and a step (f) of forming a photoelectric conversion section and an active region in the element formation regions after the step (e), wherein in the step (f) due to the width of the trench narrower than the width of the opening in the protection film, the photoelectric conversion section and the active region are arranged apart from the element isolation region, as recited in claim 70.

Inoue merely describes a fabricating process for forming a CMOS image sensor. Inoue at col. 4, paragraph [43]. Referring to FIGS. 4A and 4B, the fabricating process includes first forming a trench isolation region (56) in desired positions on a silicon substrate (51). Inoue at col. 4, paragraph [44]. Next, mask members (71) are provided on silicon substrate (51) in desired positions for forming element-isolating diffusion layers (57). Assuming, *arguendo*, that the alleged trench isolation region (56) and the alleged element-isolation diffusion layer (57) are similar to the trench and the element-isolation region, recited in claim 70, Inoue still fails to

describe or suggest forming the trench and the element-isolation region in a manner described in claim 70.

That is, Inoue fails to describe or suggest a method for manufacturing a solid-state imaging device that includes, among other steps, a step (b) of forming a sidewall on a side face of the opening in the protection film; and a step (c) of forming a trench in the element isolation formation region in the semiconductor substrate by etching using the protection film and the sidewall as a mask; a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c); a step (e) of forming an element isolation region by burying the trench with a burying film after the step (d); and a step (f) of forming a photoelectric conversion section and an active region in the element formation regions after the step (e), wherein in the step (c) the width of the trench is made smaller by the thickness of the sidewall than the width of the opening in the protection film, and in the step (f), due to the width of the trench narrower than the width of the opening in the protection film, the photoelectric conversion section and the active region are arranged apart from the element isolation region, as recited in claim 70.

Furthermore, referring to FIG. 4B and paragraph [49] of Inoue, the element-isolating diffusion layers (57) is formed so as to cover the trench isolation region 56. So, the width of the element-isolating diffusion layers 57 is wider than that of the trench isolation region 56. As such, unlike claim 70, Inoue cannot achieve the element isolation miniaturizing.

The Office Action concedes that Inoue is deficient in this regard. See e.g., the Office Action at page 3, lines 14-15 (stating that Inoue does not disclose the specific steps (a)-(d) in forming the trench isolation regions). The Office Action, however, relies on Ishizuka to remedy this shortcoming. Ishizuka is equally deficient.

The Examiner states that Ishizuka discloses in the abstract, the trench formation steps of the present invention. Applicants disagree. In particular, Ishizuka fails to describe or suggest the steps (d) and (f) of claim 70 of the present invention, and its feature, "due to the width of the trench narrower than the width of the opening, the photoelectric conversion section and the active region are arranged apart from the element isolation region."

The step (d) of claim 70 includes oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c). In contrast, in Ishizuka, a thermal oxide film (4) is formed after, a CVD oxide film (9) is removed. Therefore, step (d) of claim 70 is not disclosed in Ishizuka. Since, Ishizuka fails to describe or suggest step (d) of claim 70, it cannot describe or suggest step (f), which is performed after step (d).

Furthermore, as shown in FIG. (e) of Ishizuka, a top edge of the oxide film (4) is formed by oxidization of the top edge of a trench. The top edge of the oxide film (4) is formed between the top surface of a silicon substrate (1) and a silicon nitride film (5) and hence, the top edge of the oxide film (4) is formed so as to spread from the trench to the element formation region on the top surface of the silicon substrate (1). Therefore, unlike in claim 70, it is difficult for Ishizuka to make the element isolation miniaturized.

Accordingly, Inoue and Ishizuka, either alone or in combination, fail to describe or suggest a method for manufacturing a solid-state imaging device that includes, among other steps, a step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c) and a step (f) of forming a photoelectric conversion section and an active region in the element formation regions after the step (e), wherein in the step (f) due to the width of the trench narrower than the width of the

opening in the protection film, the photoelectric conversion section and the active region are arranged apart from the element isolation region, as recited in claim 70.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 70 along with its dependent claims.

Claim 77 relates to a solid-state imaging device fabricated by the method recited in claim 70. Therefore, for at least the reasons presented above with respect to claim 70, Applicants respectfully submit that Inoue and Ishizuka, either alone or in combination, do not describe or suggest the structure of claim 77.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 77 along with its dependent claims.

Dependent Claims

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Because claims 70 and 77 are allowable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also allowable. In addition, it is respectfully submitted that the dependent claims are allowable based on their own merits by adding novel and non-obvious features to the combination.

For example, claim 81 recites a method for manufacturing a solid-state imaging device that includes, among other steps, a step of implanting a p-type ion into a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c) and before the step (d) (emphasis added). The Office Action asserts that Houston

teaches this feature in column 6, lines 7-64. Applicants disagree. To this end, Applicants submit that in FIG. 5 and col. 6, lines 14-29, Houston describes performing implantation after the sidewalls are removed. Therefore, Houston in this portion fails to describe or suggest the above-recited feature.

For at least this reason and the reasons presented above with respect to claim 70, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 81.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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